

1 Claims

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3 1. Device for equalizing the charge of the serially connected
4 capacitors belonging to a double layer capacitor (DLC),
5 with one capacitor (C1 to Cn) in each case being assigned a
6 single transformer (Tr1 to Trn) in each case whose
7 secondary winding is connected by way of a single diode (D1
8 to Dn) to the positive terminal of the capacitor and
9 directly to the negative terminal, and to a voltage
10 comparator,

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14 in that a flyback transformer (Tr0) is provided whose primary
15 and secondary windings are wound in phase-opposition to one
16 another, whereby the end of winding of its primary winding
17 is connected to the positive terminal (V+) of the double
18 layer capacitor (DLC) and the start of winding is connected
19 to the collector or drain terminal of a switching
20 transistor (T1),

21 in that the end of winding of the secondary winding of the
22 flyback transformer (Tr0) is connected directly to the
23 negative terminal (V-) of the double layer capacitor (DLC),
24 while the start of winding is connected by way of the
25 series connection of a first diode (D0) and a second
26 resistor (R2) to the negative terminal (V-) of the double
27 layer capacitor (DLC),

28 in that a first voltage comparator (KOMP1) is provided whose
29 inverting input is connected on the one hand to the emitter
30 or source terminal of the switching transistor (T1) and on
31 the other hand to a first resistor (R1) whose other
32 terminal is connected to the negative terminal (V-) of the
33 double layer capacitor (DLC),

1 in that a first AND element (UND1) is provided whose output
2 is connected to the base or gate terminal of the switching
3 transistor (T1) and to whose one input an external control
4 signal (EN) is fed,
5 in that a second AND element (UND2) is provided whose output
6 is connected to the other input of the first AND element
7 (UND1), and whose one input is connected to the output of
8 the first voltage comparator (KOMP1),
9 in that a second voltage comparator (KOMP2) is provided whose
10 inverting input is connected to the connection point
11 between the first diode (D0) and the second resistor (R2),
12 in that a first reference voltage (Vref1) is provided which
13 is applied to the noninverting inputs of the first (KOMP1)
14 and second voltage comparator (KOMP2),
15 in that the output of the second voltage comparator (KOMP2)
16 is connected to the other input of the second AND element
17 (UND2),
18 in that a monitoring unit (DIAG) is provided whose first
19 input is connected to the output of the first voltage
20 comparator (KOMP1), whose second input is connected to the
21 output of the second voltage comparator (KOMP2), whose
22 third input is connected to the inverting input of the
23 second voltage comparator (KOMP2), at whose fourth input a
24 second reference voltage (Vref2) is applied, and at whose
25 output a status signal (ST) can be taken off,
26 in that the single transformers (Tr1 to Trn) are wound in-
27 phase, whereby the start of winding of the secondary
28 winding of each single transformer (Tr1 to Trn) is
29 connected by way of a single diode (D1 to Dn) to the
30 positive terminal of the single capacitor (C1 to Cn)
31 assigned to it, while its end of winding is connected
32 directly to the negative terminal of the single capacitor
33 (C1 to Cn) assigned to it,

1 in that the primary windings of the single transformers (Tr1
2 to Trn) are connected in parallel, whereby the common start
3 of winding is connected to the connection point between the
4 first diode (D0) and the second resistor (R2) and the
5 common end of winding is connected to the negative terminal
6 (V-) and to the end of winding of the secondary winding of
7 the flyback transformer (Tr0).

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9 2. Device for equalizing the charge of the serially connected
10 capacitors belonging to a double layer capacitor (DLC),
11 with each capacitor (C1 to Cn) being assigned a single
12 transformer (Tr1 to Trn) in each case whose secondary
13 winding is connected by way of a single diode (D1 to Dn) to
14 the positive terminal of the capacitor and directly to the
15 negative terminal, and to a voltage comparator,

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19 in that an inductor (L1) is provided whose one terminal is
20 connected to the positive terminal (V+) of the double layer
21 capacitor (DLC) and whose other terminal is connected on
22 the one hand to the collector or drain terminal of a
23 switching transistor (T1),

24 in that a PNP transistor (T2) is provided whose base terminal
25 is connected to the one terminal of the inductor (L1),
26 whose emitter terminal is connected by way of a third
27 resistor and a first diode (D0) to the other terminal of
28 the inductor (L1), and whose collector terminal is
29 connected by way of a second resistor to the negative
30 terminal (V-) of the double layer capacitor (DLC),

31 in that a first voltage comparator (KOMP1) is provided, whose
32 inverting input is connected on the one hand to the emitter
33 or source terminal of the switching transistor (T1) and on

1 the other hand to a first resistor (R1), whose other
2 terminal is connected to the negative terminal (V-) of the
3 double layer capacitor (DLC),
4 in that a first AND element (UND1) is provided whose output
5 is connected to the base or gate terminal of the switching
6 transistor (T1) and to whose one input an external control
7 signal (EN) is supplied,
8 in that a second AND element (UND2) is provided whose output
9 is connected to the other input of the first AND element
10 (UND1) and whose one input is connected to the output of
11 the first voltage comparator (KOMP1),
12 in that a second voltage comparator (KOMP2) is provided whose
13 inverting input is connected to the connection point
14 between the collector of transistor (T2) and the second
15 resistor (R2),
16 in that a first reference voltage (Vref1) is provided which
17 is applied to the noninverting inputs of the first (KOMP1)
18 and second voltage comparator (KOMP2),
19 in that the output of the second voltage comparator (KOMP2)
20 is connected to the other input of the second AND element
21 (UND2),
22 in that a monitoring unit (DIAG) is provided whose first
23 input is connected to the output of the first voltage
24 comparator (KOMP1), whose second input is connected to the
25 output of the second voltage comparator (KOMP2), whose
26 third input is connected to the inverting input of the
27 second voltage comparator (KOMP2), at whose fourth input a
28 second reference voltage (Vref2) is applied, and at whose
29 output a status signal (ST) can be taken off,
30 in that the single transformers (Tr1 to Trn) are wound in-
31 phase, whereby the start of winding of the secondary
32 winding of each single transformer (Tr1 to Trn) is
33 connected by way of a single diode (D1 to Dn) to the

1 positive terminal of the single capacitor (C1 to Cn)
2 assigned to it, while its end of winding is connected
3 directly to the negative terminal of the single capacitor
4 (C1 to Cn) assigned to it, and
5 in that the primary windings of the single transformers (Tr1
6 to Trn) are connected in parallel, whereby the common start
7 of winding is connected to the connection point between the
8 first diode (D0) and the third resistor (R3) and the common
9 end of winding is connected to the positive terminal (V+)
10 of the double layer capacitor (DLC) and to the one terminal
11 of the inductor (L1).

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13 3. Device according to Claim 1 or 2, characterized in that
14 the single transformers (Tr1 to Trn) and the single diodes D1
15 to Dn are located together with the single capacitors (C1 to
16 Cn) in the housing of the double layer capacitor (DLC).

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18 4. Device according to Claim 1 or 2, characterized in that
19 the connection between the flyback transformer (Tr0) or the
20 inductor (L1) and the single transformers is implemented by
21 means of a two-wire bus cable.

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23 5. Device according to Claim 1, characterized in that a first
24 capacitor (C0) is provided, which is connected on the one
25 hand to the cathode terminal of the first diode (D0) and on
26 the other hand to the negative terminal (V-).

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28 6. Device according to Claim 2, characterized in that a first
29 capacitor (C0) is provided, which is connected on the one
30 hand to the cathode terminal of the first diode (D0) and on
31 the other hand to the positive terminal (V+).

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33 7. Method for operating the device according to Claim 1 or 2,

1 characterized in that the operation takes place in self-
2 controlled fashion, whereby switching transistor (T1)
3 is made conducting as soon as an external control signal (EN)
4 is present and as soon as the voltage at the secondary
5 winding of the flyback transformers (Tr0) or at the
6 inductor (L1) lies beneath a predefined value,
7 is made nonconducting when the current flowing through the
8 primary winding of the flyback transformer (Tr0) or through
9 the inductor (L1) reaches a predefined value, and
10 remains nonconducting as long as the voltage at the secondary
11 winding of the flyback transformer (Tr0) or at the inductor
12 (L1) exceeds a predefined value or the external control
13 signal (EN) is not present.

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15 8. Method according to Claim 1 or 2, characterized
16 in that the signal duration, corresponding to the charging
17 time, which can be measured at the output of the first
18 voltage comparator (KOMP1) and the signal duration,
19 corresponding to the discharging time of the flyback
20 transformer (Tr0) or of the inductor (L1), which can be
21 measured at the output of the second voltage comparator
22 (KOMP2) are in each case compared with an upper and a lower
23 limit value in the monitoring circuit (DIAG), and
24 in that it is assumed that the double layer capacitor (DLC)
25 and the charge equalizing circuit are in a perfect state as
26 long as the measured values lie within the limit values,
27 and
28 in that the monitoring circuit (DIAG) issues a status signal
29 (ST) corresponding to this state.

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31 9. Method according to Claim 1 or 2, characterized in that
32 the amplitude of the rectified discharging voltage, which can
33 be measured during a discharging operation of the flyback

1 transformer (Tr0) or of the inductor (L1) after the transient
2 reaction, is proportional to the currently lowest voltage of
3 a single capacitor (C1 to Cn) of the double layer capacitor
4 (DLC).

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6 10. Method according to Claim 8 or 9, characterized
7 in that the amplitude of the rectified discharging voltage,
8 which can be measured after the transient reaction, is in
9 each case compared with an upper and a lower limit value in
10 the monitoring circuit (DIAG),
11 in that it is assumed that the double layer capacitor (DLC)
12 is in a perfect state as long as the measured values lie
13 within the limit values, and
14 in that the monitoring circuit (DIAG) issues a status signal
15 (ST) corresponding to this state.

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